Foundries: CORNERSTONE

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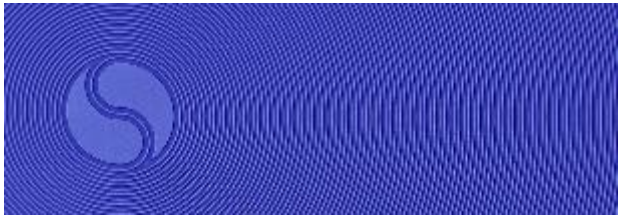
G. T. Reed (University of Southampton, UK)

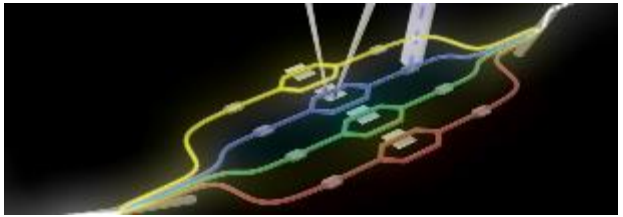
G. Sharp, M. Sorel (University of Glasgow, UK)

J. England, R. Webb (University of Surrey, UK)

CORNERSTONE - Overview

- CORNERSTONE: CAPABILITY FOR OPTOELECTRONICS, METAMATERIALS, NANOTECHNOLOGY AND SENSING
- EPSRC-funded project (2014-2019) with a total budget of £3.2 million
- Goal: to establish silicon photonics fabrication capability that can support photonics research in the UK via MPW service
- Vision: to underpin photonics research in UK and support wide range of research activities, attracting both academic and commercial partners



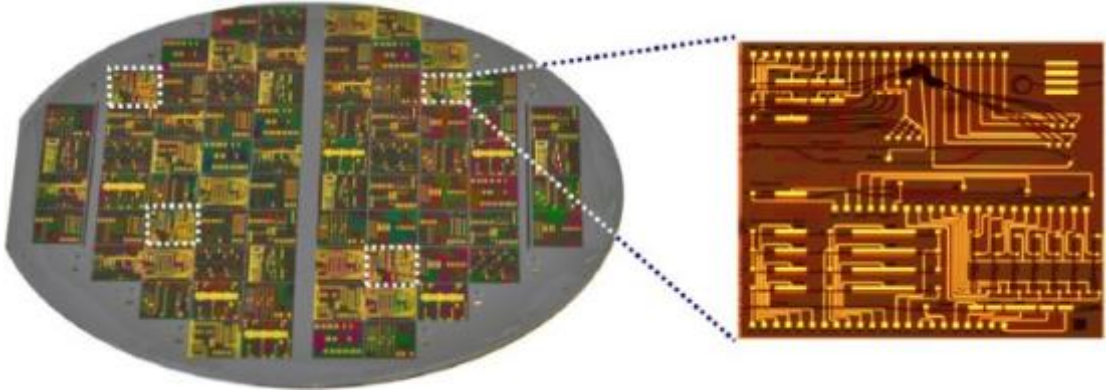


CORNERSTONE rationale

- Uses industry compatible DUV lithography (the only such capability in UK academia)
  - Enables seamless scaling to higher volumes
- Increases utilization of advanced cleanroom technology in the UK
- Builds on capability developed in other EPSRC funded research projects in Southampton, Glasgow and Surrey
- Shares knowledge and expertise with partner Universities in UK
- More appealing to industry

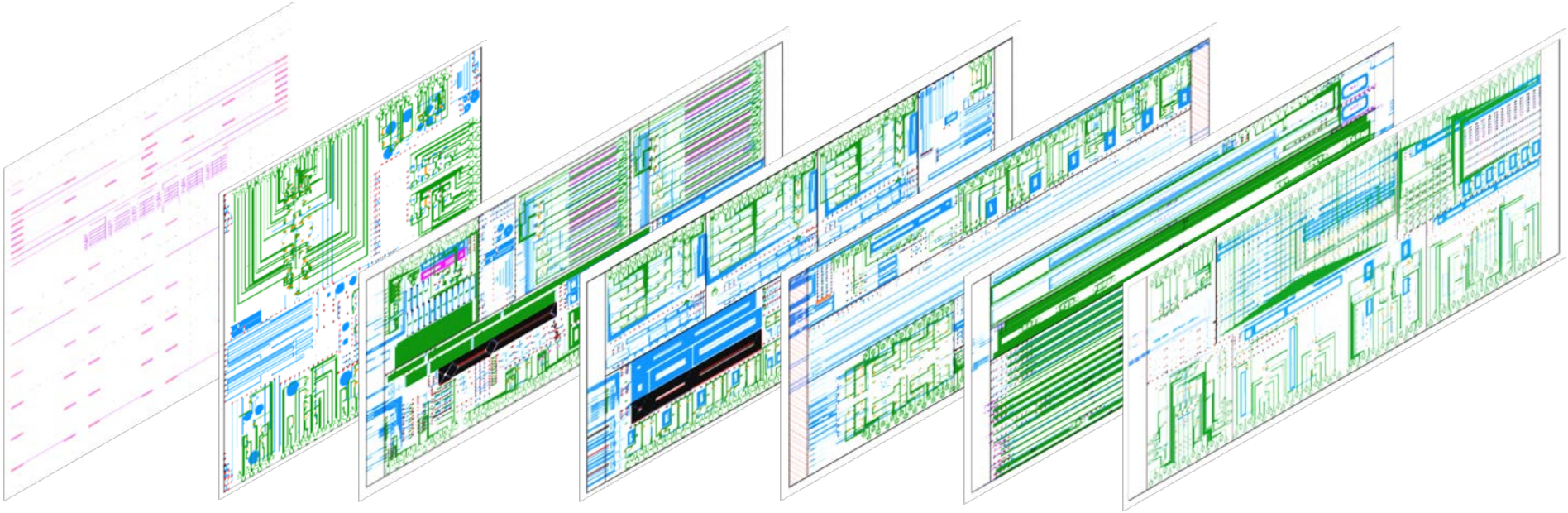
Multi-project-wafer capability

- Cost sharing mechanism to improve accessibility to advanced technology:
  - Fixed design rules and processed announced every 2 months
  - Designs from various designers processed together on the same wafer
  - Wafer ‘sliced’ up once processing is complete



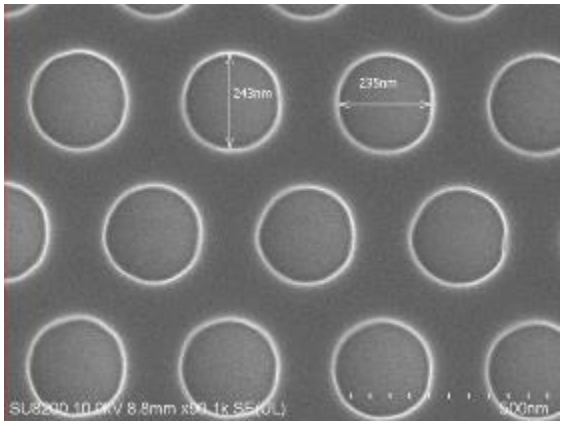
Bristol PG collaboration with CORNERSTONE

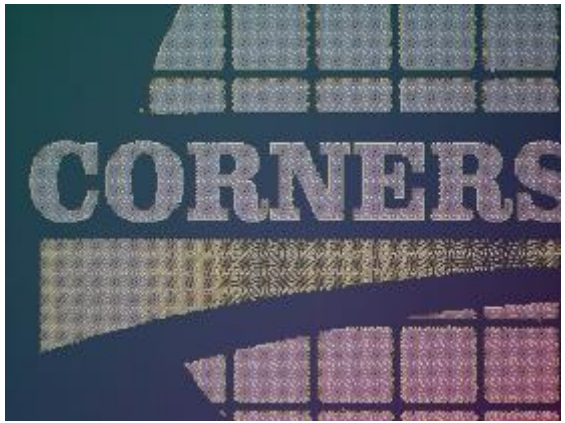
- Bristol PG interaction with CORNERSTONE:
  - Submitted at least 1 cell to 10 of the 12 CORNERSTONE calls to date

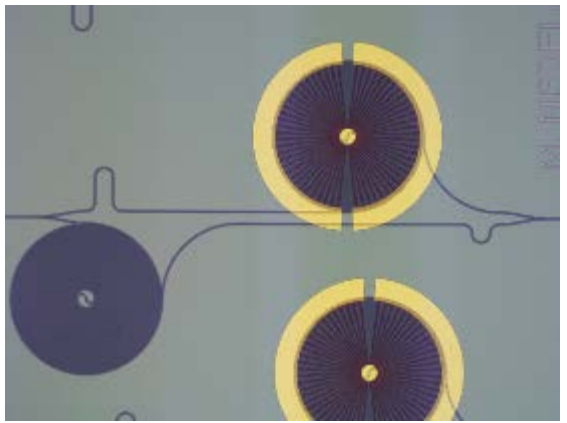


Bristol PG collaboration with CORNERSTONE

- Number of cells submitted: **20**
- Number of chips provided by CORNERSTONE: **137**
- Number of chips under fabrication: **74**
- Total value of chips (provided for free under EPSRC funding): **£325k**

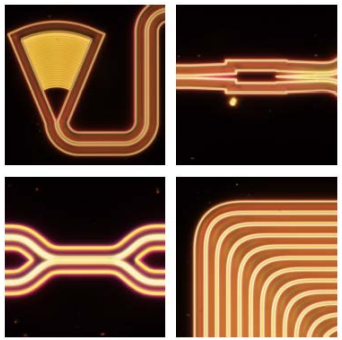


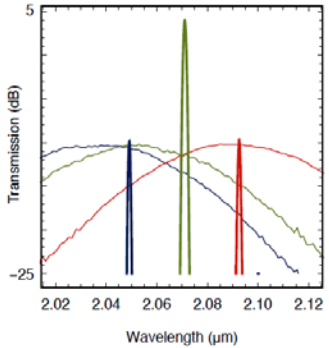




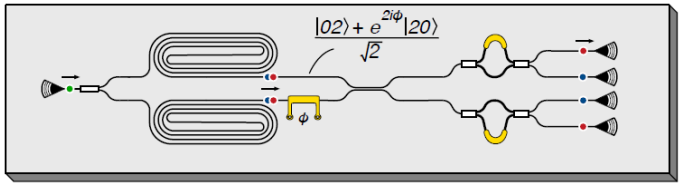
Case studies

SWIR quantum photonics

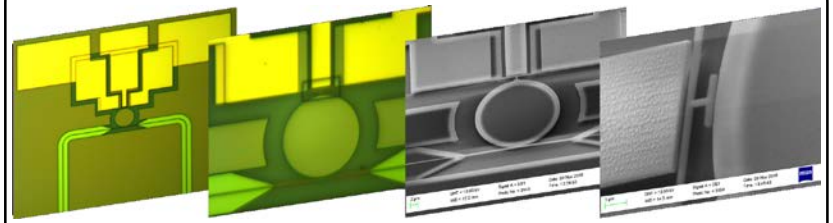




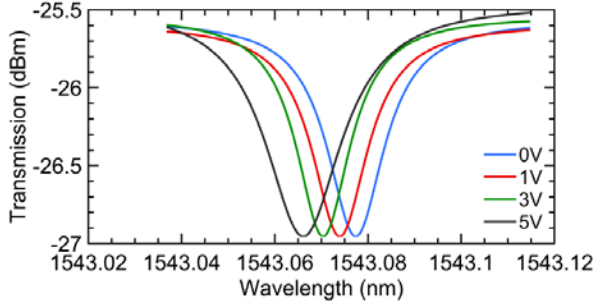
- Quantum interference demonstrated in the SWIR (λ = 2 μm)



MEMS modulators



- Silicon processing through CORNERSTONE
- Post processed at Bristol to add MEMS layers

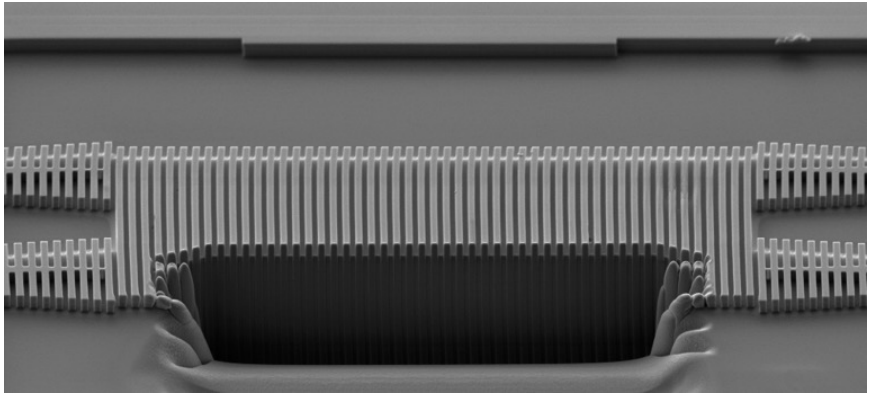


CORNERSTONE partners

- Three UK universities are involved:
  1) University of Southampton
     (Prof. Graham Reed)
     - Wafer-scale processing (DUV photolithography)
  2) University of Glasgow
     (Prof. Marc Sorel)
     - Chip-level processing (e-beam lithography)
  3) University of Surrey
     (Prof. Jonathan England)
     - Ion implantation

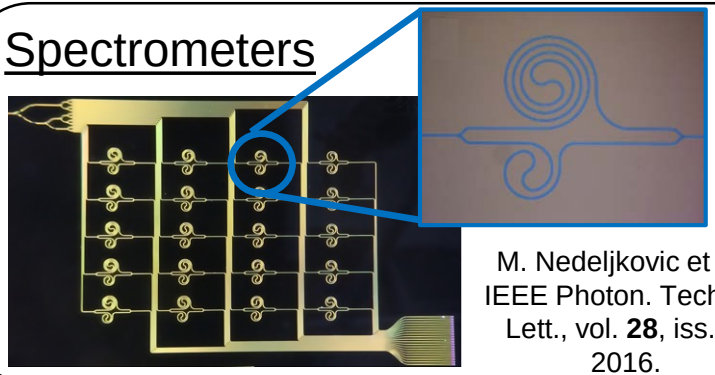
What is offered?

- 3x SOI platforms:
  - ➢220 nm Si on 2 µm BOX
  - ➢340 nm Si on 2 µm BOX
  - ➢500 nm Si on 3 µm BOX
- Passive device fabrication runs:
  - ➢Waveguides, MUX, DEMUX, filters,...
- Passive device with heaters fabrication runs:
  - ➢Tunable MZI, tunable filters,...
- Active device fabrication runs:
  - ➢Modulators,...



Example device capabilities

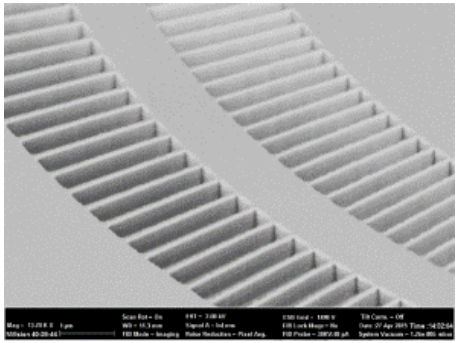
Spectrometers



M. Nedeljkovic et al., IEEE Photon. Technol. Lett., vol. **28**, iss. 4, 2016.

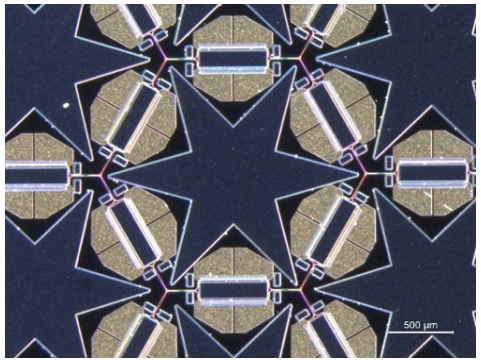
Suspended waveguides

G. Z. Mashanovich et al., J. Sel. Top. Quantum Electron., vol. **21**, iss. 4, 2015.



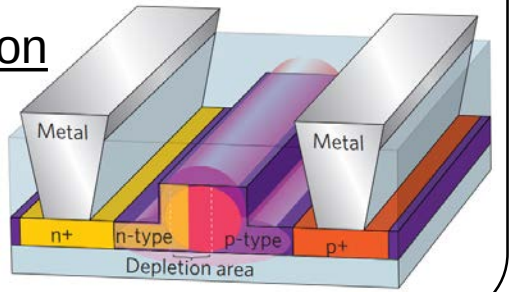
Tuneable processor cores

D. Pérez et al., Nat. Commun., vol. **8**, 636, 2017.



High speed carrier depletion modulators

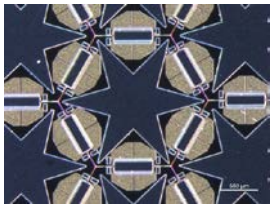
G. Reed et al., Nat. Photonics, vol. **4**, pp. 518–526, 2010.

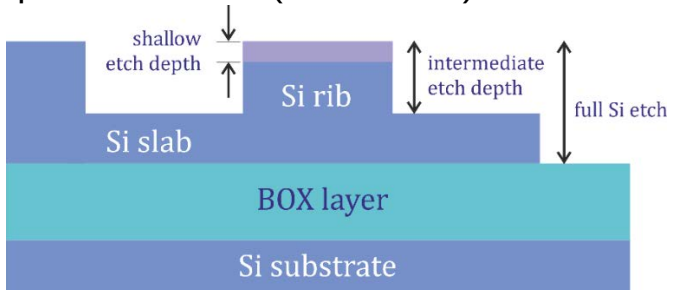


MPW call types

Passive devices (with heaters)

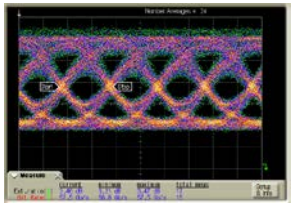
- Up to 3 silicon etch depths
- 2 metal layers for heaters
- Various SOI platforms
- Rapid turn-around (< 3 months)

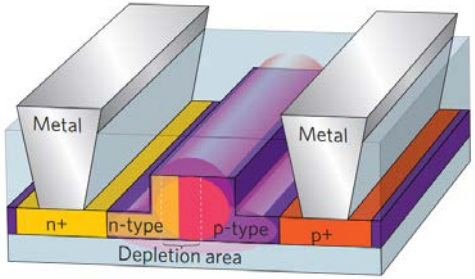




Active devices

- Up to 3 silicon etch depths
- 4 implantation levels
- 1 metal layer for electrodes
- 220 nm SOI platform



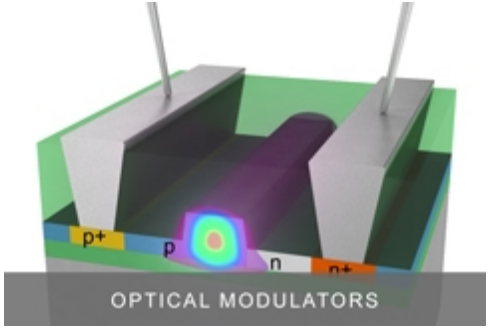


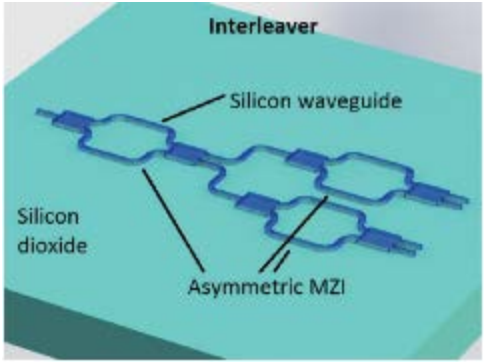
Design rules, PDK, terms and conditions etc. available on the CORNERSTONE website: www.cornerstone.sotonfab.co.uk

2019 schedule

Call	Call Type	Feb. 2019	Mar. 2019	Apr. 2019	May. 2019	Jun. 2019	Jul. 2019	Aug. 2019	Sep. 2019	Oct. 2019	Nov. 2019	Dec. 2019	Jan. 2020	Feb. 2020
MPW #12 – 340 nm SOI platform	Passive													
MPW #13 – 220 nm SOI platform	Passive													
MPW #14 – 500 nm SOI platform	Passive													
MPW #15 – 220 nm SOI platform	Passive				Call announced →							← Submission deadline		
MPW #16 – 340 nm SOI platform	Passive													
MPW #17 – 220 nm SOI platform	Active													
MPW #18 – 220 nm SOI platform	Passive													

*Schedule is subject to change

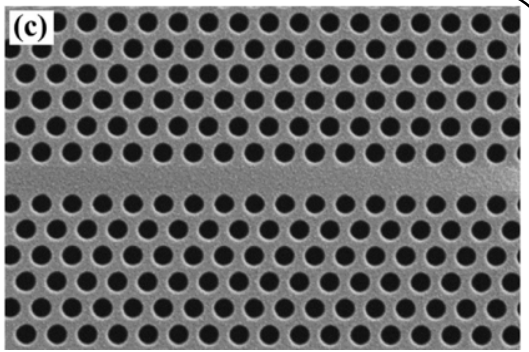




Schedule on our website: www.cornerstone.sotonfab.co.uk

CORNERSTONE 2 proposal (in progress)

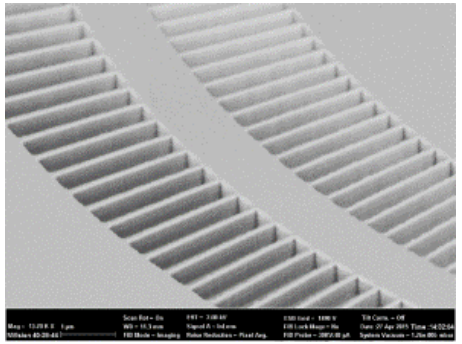
Silicon nitride



Applications:

- Low-loss passive Si photonics
- Visible wavelengths
- Quantum photonics

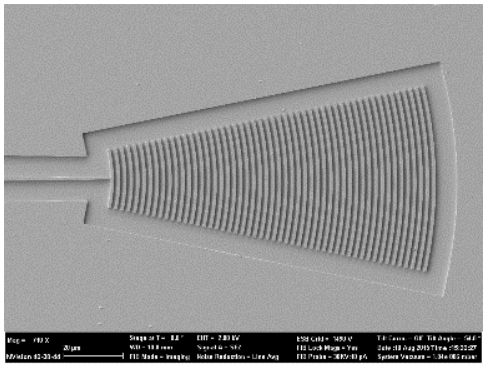
Suspended waveguides



Applications:

- Mid-IR sensing
- MEMS/MOEMS

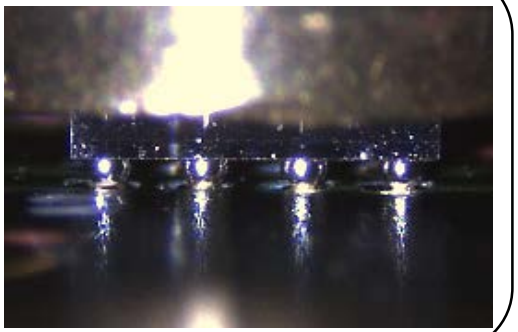
Germanium -on-Silicon



Applications:

- Mid-IR silicon photonics
- Sensing

EIC bonding and III-V pick and place



Applications:

- Integrated transceivers
- Light sources and detectors